Umutcan Akyol

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Github Profile

I am someone who truly enjoys working with computers and keeps learning every day. I spend most of my time learning new stuff and **making projects** mostly. I can work with different kinds of technologies.

Work Experience

Arcelik Global A.S, Istanbul/Turkey - Intern

07/23 - 10/23

For a short time I worked as an intern at Arcelik global in the Merchandising department. Through this experience, I learned to work efficiently and understood the importance of idea exchange in teamwork. Also, I realized how crucial human relations are for collaboration with colleagues.

Education

Duzce University, Duzce/Turkey

09/24 - *

As of now, I am studying at Duzce University in Computer Engineering as a student. Before that I was a student at Gaziantep University in Mechanical Engineering. But that was not a subject I was interested in. That is why I dropped out of that faculty.

Projects

ChaCha20 RTL and ASIC design with OpenLane and SkyWater 130nm PDK:

I designed and implemented the ChaCha20 stream cipher RTL module from scratch using Verilog HDL. Executed the complete RTL-to-GDSII digital implementation flow utilizing the open-source OpenLane compiler and SkyWater 130nm PDK. This project enhanced my HDL design capabilities and provided deep practical expertise in cryptographic hardware architectures, digital logic synthesis, and physical design constraints.
ChaCha20 Github Page

RTOS Core design and implementation for STM32XX Devices:

Designed and implemented a lightweight, modular Real-Time Operating System (RTOS) kernel from scratch to support custom embedded projects. Developed the core preemptive task scheduler, task control blocks (TCBs), and context-switching mechanisms to handle real-time task execution efficiently. This project deepened my expertise in low-level systems programming, CPU architecture, interrupt handling, and bare-metal hardware integration.
RTOS Core Github Page

Abilities

C/C++ Programming

Embedded Programming

RTOS Development

VHDL

Verilog

Asic Front End Design

VLSI Design and Verification

Python

Arm Architecture and Assembly

x86 Assembly

Java / Java EE

Java Spring Framework

Unity

Git/Github

Linux

Languages

English(>=B2),

German(A1),

Chinese(HSK2)

Tiny Encryption Algorithm Implementation for FPGA's:

Designed and implemented the Tiny Encryption Algorithm (TEA) pipeline architecture utilizing Verilog HDL. Developed modular hardware blocks optimized for hardware efficiency and cryptographic throughput, and validated the design's functionality via comprehensive testbench simulations. This project strengthened my skills in FPGA prototyping, hardware description languages, and data security integration.
TEA Github Pag